Application No.: 10/640,349   Docket No.: JCLA11051-R

In The Claims:

Please amend the claims as follows:

Claim 1. (currently amended)   A graphics display method for continuously displaying <u>a</u> <u>plurality of</u> graphics data on multiple display devices of a computer <u>system</u> that contains <u>a</u> <u>central processing unit (CPU) which has a memory controller inside, a graphics-processing unit</u> <u>coupled to the memory controller, and</u> a system memory directly accessed by [[a]]<u>the CPU,</u> <u>wherein the display devices are coupled to the graphics-processing unit</u>, the method comprising:

providing a common clock source to the display devices and using [[a]]<u>the</u> common clock source to synchronize <u>a plurality of</u> blank periods of the display devices;

receiving a power saving signal from the CPU, [[said]]<u>the</u> power saving signal indicates a request for executing a power saving process by the CPU during a[[n]] non-responding period <u>of</u> <u>the CPU, so as to reduce power consumption of the CPU, wherein memory access from the</u> <u>graphics-processing unit to the system memory is blocked during the non-responding period of</u> <u>the CPU</u>; and

executing the power saving process within [[the]]<u>a</u> least common multiple occurrence of the blank periods of the display devices.

Claim 2. (currently amended)   The method of claim 1<u>,</u> further comprising a step of detecting the upcoming least common multiple occurrence of the blank periods of the display devices before [[the]] executing [[step]]<u>the power saving process</u>.

Claim 3. (currently amended)   The method of claim 1<u>,</u> wherein the blank period<u>s</u> can be a <u>plurality of</u> horizontal blank period<u>s</u> (HBP<u>s</u>) or a <u>plurality of</u> vertical blank period<u>s</u> (VBP<u>s</u>).

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Claim 4. (currently amended)   The method of claim 3, wherein the horizontal blank

periods or the vertical blank periods [[is]]are provided by [[a]]the graphics-processing unit.

Claims 5-16 (cancelled)

Claim 17. (currently amended) A graphics display method for continuously displaying a

plurality of graphics data on multiple display devices of a computer system that contains a

central processing unit (CPU) which has a memory controller inside, a graphics-processing unit

coupled to the memory controller, and a system memory directly accessed by [[a]]the CPU,

wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using [[a]]the common

clock source to synchronize blank periods of the display devices;

receiving a power saving signal from the CPU, [[said]]the power saving signal indicates a

request for executing a power saving process [[by]]to make the CPU self-adjust self-adjusting a

CPU frequency clock rate and a power level of the CPU during a[[n]] non-responding period of

the CPU, wherein memory access from the graphics-processing unit to the system memory is

blocked during the non-responding period of the CPU; and

executing the power saving process within [[the]]a least common multiple occurrence of

the blank periods of the display devices.

Claim 18. (currently amended) The method of claim 17, wherein while executing the

power saving process, the system memory is continuously accessed by the CPU during the

non-responding period of the CPU.

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In The Drawings:

Please substitute the attached clean sheets of drawings of Figs. 3 and 4 for the original drawings of Figs. 3 and 4. Compared with the original FIG. 3, the reference characters "32", "33", "35", "36", "37", "39", and "40" are cancelled in the amended FIG. 3. Compared with the original FIG. 4, the reference characters "37", "39", "40", "42", "43", "45", and "50" are cancelled in the amended FIG. 4.